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EXAMINER	
TSENG, CHENG YUAN	
ART UNIT	**PAPER NUMBER**
2184	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/736,125	PAI ET AL.	
	Examiner	Art Unit	
	CHENG-YUAN TSENG	2184	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 March 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *18-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *18-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The objections to specification, and claim rejections made under 35 U.S.C. 112 have been withdrawn due to the amendment filed on March 4, 2010.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless – (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 18-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Lee (U.S. Patent 6,842,219), hereinafter referred to as Lee.

Referring to claim 18, Lee discloses **a direct memory access controller** (fig. 2, decoding processor 201 with DMA units), said direct memory access controller comprising:

a state logic machine (fig. 4, decoding sequencing control unit DSCU 203a; fig. 2, DSCU 203a; fig. 9, state transition of DSCU 203a; note, each arc of the diagram represents a command for transition to another state) for **receiving a single command** (fig. 4, receiving commands from RISC interface 401; col. 10, lines 33-36, data/address/control signals from RISC; fig. 6, coprocessor command for DSCU; col. 4, lines 27-29) to provide **a specified range** (col. 11, lines 15-19, address range of external memory to be accessed; col. 4, lines 27-29, coprocessor command of access external memory) of **a plurality of sequential data words** (col. 11, lines 62-65, DSCU carries sequential sequence control of MPEG stream; col. 12, lines 38-41, for example, macroblock as data words), wherein the single command expressly states **a starting address** (col. 10, lines 41-46, start address to be used; col. 13, lines 45-52, initial start location of the bus stream) and **an ending address** (col. 10, lines 41-46, end address of the memory to be used; col. 13, lines 45-52, the location of the bit stream up to which decoding is completed) of said specified range; and

a memory controller (fig. 11, buffer controller 1113 of variable length decoder VLD 203ba; fig. 2, VLD 203ba; fig. 12, reversal logic) for fetching **a first portion** (fig. 11, a portion of VLD input buffer 1112; col. 13, lines 27-35, fetch into barrel shift 1104 to lower 32 bit) of the specified selectable range and **a second portion** (fig. 11, a next portion of VLD input buffer 1112; col. 13, lines 27-35, move lower 32 bit to higher 32 and fetch new lower 32 bit) of the specified selectable range after fetching the first portion, wherein the second portion of the range has **a lower address than** (col. 13, lines 27-35, barrel shifter 1104, the new fetch is always shift into lower 32 bit address) the first portion, after the state logic receives the single command including the starting address and the ending address.

Referring to claim 24, Lee discloses a method for fetching data words, said method comprising:

receiving a single command (fig. 4, receiving commands from RISC interface 401; col. 10, lines 33-36, data/address/control signals from RISC; fig. 6, coprocessor command for DSCU; col. 4, lines 27-29) to provide **a specified range** (col. 11, lines 15-19, address range of external memory to be accessed; col. 4, lines 27-29, coprocessor command of access external memory) of **a**

plurality of sequential data words (col. 11, lines 62-65, DSCU carries sequential sequence control of MPEG stream; col. 12, lines 38-41, for example, macroblock as data words) in **a memory** (fig. 2, external memory via 215), wherein the command expressly states a starting at **a beginning address** (col. 10, lines 45-46, start address of the memory) and ending at **an ending address** (col. 10, lines 45-46, end address of the memory) of said range;

fetching a portion (col. 6, lines 58-60, four words), in **a forward address order** (col. 13, lines 33-35, increased address), of the range of **sequential data words** (col. 13, lines 33-35, bit stream), said wherein said portion of the range of sequential data words consists of **a predetermined amount of data words** (col. 6, lines 58-60, four words) that conclude with and precede the ending address, and wherein the predetermined amount of data words is equivalent to **a capacity of a local buffer** (col. 6, lines 58-60, a one line capacity of a cache memory);

storing (col. 6, lines 58-60, fill the cache memory) the predetermined amount of data words that conclude with and precede the ending address in the local buffer;

fetching, in the forward address order, at least one preceding portion (col. 13, lines 33-35, increased address) of the range of sequential data words, wherein each of the

preceding portions of the range of sequential data words consist of the predetermined amount of data words; and

wherein **a one of the preceding portions** (col. 10, lines 49-55, backward decoding; col. 15, lines 49-52, MPEG-4 rewinding and error resilience, the point of error has beginning address) of the range of sequential data words comprises the starting address, truncating those data words that precede the beginning address.

Referring to claim 30, Lee discloses **a system for decoding video data** (fig. 2, MPEG video decoding processor 201 with DMA units), said system comprising:

a memory (fig. 2, external memory via 215) for storing **a packetized elementary stream** (col. 11, lines 62-65, DSCU carries sequential sequence control of MPEG stream; col. 12, lines 38-41, for example, macroblock as data words), said packetized element stream comprising **a plurality of packets** (col. 14, lines 54-55, video packet);

a start code table (col. 10, lines 41-46, DSCU register 403 with DEC memory 203) for **storing starting addresses** (col. 10, lines 41-46, start address) and **ending addresses** (col. 10, lines 41-46, end address) of said plurality of packets;

a video decoder (fig. 2, VDEC 203) for **decoding a particular one of the plurality of packets** (col. 7, lines 12-13, current frame), wherein the video decoder **looks up** (col. 12, lines 46-49, inform DSCU to start decoding) the starting addresses and the ending addresses of the particular one of the plurality of packets and **issues a single command** (fig. 4, receiving commands from RISC interface 401; col. 10, lines 33-36, data/address/control signals from RISC; fig. 6, coprocessor command for DSCU; col. 4, lines 27-29) to fetch the packet, wherein the single command expressly includes **a starting address** (col. 10, lines 41-46, start address to be used; col. 13, lines 45-52, initial start location of the bus stream) and **an ending address** (col. 10, lines 41-46, end address of the memory to be used; col. 13, lines 45-52, the location of the bit stream up to which decoding is completed) associated with the particular one of the plurality packets; and

a direct memory access controller (fig. 2, decoding processor 201 with DMA units), said direct memory access controller comprising:

a state logic machine (fig. 4, decoding sequencing control unit DSCU 203a; fig. 2, DSCU 203a; fig. 9, state transition of DSCU 203a; note, each arc of the diagram represents a command

for transition to another state) for receiving the single command; and

a memory controller (fig. 11, buffer controller 1113 of variable length decoder VLD 203ba; fig. 2, VLD 203ba; fig. 12, reversal logic) for **fetching a first portion** (fig. 11, a portion of VLD input buffer 1112; col. 13, lines 27-35, fetch into barrel shift 1104 to lower 32 bit) of **a range** (col. 11, lines 15-19, address range of external memory to be accessed; col. 4, lines 27-29, coprocessor command of access external memory), said range comprising **sequential data words** (col. 11, lines 62-65, DSCU carries sequential sequence control of MPEG stream; col. 12, lines 38-41, for example, macroblock as data words) from the starting address to the ending address for the particular one of the plurality of packets, and **a second portion** (fig. 11, a next portion of VLD input buffer 1112; col. 13, lines 27-35, move lower 32 bit to higher 32 and fetch new lower 32 bit) of the range after fetching the first portion, wherein the second portion of the range has **a lower address than the first portion** (col. 13, lines 27-35, barrel shifter 1104, the new fetch is always shift into lower 32 bit address), after the state logic receives the single command including the starting address and the ending address.

As to claim 19, Lee discloses the direct memory access controller of claim 18, wherein the memory controller fetches the first portion of the range and the second portion of the range in **a forward address order** (col. 13, lines 33-35, increased address).

As to claim 20, Lee discloses the direct memory access controller of claim 18, further comprising: **a local buffer** (col. 6, lines 58-60, the cache memory; and fig. 16, DBC MEM) for storing the first and second portions in **a forward address order** (col. 13, lines 33-35, increased address), said local buffer comprising **a plurality of data words** (fig. 16, DBC MEM, four words).

As to claim 21, Lee discloses the direct memory access controller of claim 20, wherein the plurality of data words of the local buffer are **narrower in width** (fig. 16, DBC MEM with 16 bytes vs. input stream in words) than the sequential data words.

As to claim 22, Lee discloses the direct memory access controller of claim 20, further comprising: **a port** (fig. 12, PMU IN) for transmitting the contents of the plurality of data

words of the local buffer in **a reverse address order** (fig. 12, reversal logic).

As to claim 23, Lee discloses the direct memory access controller of claim 22, further comprising: **at least one multiplexer** (fig. 12, multiplexers inside 1203) for reversing the bit positions of contents of **at least one of the data words** (fig. 12, B DO[31:0]) of the local buffer.

As to claim 25, Lee discloses the method of claim 24, further comprising: **loading** (fig. 12, load into CLUST DEC 1202) the portion and the at least one preceding portions of the sequential data words into the local buffer.

As to claim 26, Lee discloses the method of claim 25, further comprising: **reversing** (fig. 12, reversal logic) the portion and the at least one preceding portions of the range of sequential data words.

As to claim 27, Lee discloses the method of claim 26, further comprising: **reversing** (col. 10, lines 49-55, backward decoding; col. 15, lines 49-52, MPEG-4 rewinding and error resilience, the point of error has beginning address) the

truncated one of the preceding portions of the range of sequential data words that comprises the beginning address.

As to claim 28, Lee discloses the direct memory access controller of claim 18, wherein the first portion and the second portion are **adjacent to each other** (fig. 14, bit stream forms the first/second portions, stream has adjacent bits).

As to claim 29, Lee discloses the direct memory access controller of claim 18, wherein the specified selectable range of the plurality of sequential data words is **less than** (col. 11, lines 15-19, address range of external memory to be accessed is less than the external memory range) **a memory** (fig. 2, external memory via 215) storing the plurality of sequential data words.

Response to Arguments

4. Applicant's arguments filed on March 4, 2010, regarding the 35 U.S.C. §102 have been fully considered, but they are not deemed to be persuasive.

Applicant argues that Lee does not disclose "wherein the single command expressly states a starting address and an ending

address of said specified range" in amended independent claims, and indicates Lee's command discloses range (pages 1-2).

Examiner disagrees with applicant, because a given range must have associated starting and ending addresses. Furthermore, Lee expressively discloses DSCU register 403 and DEC memory 203 for start address and the end address of the memory to be used (col. 10, lines 41-46).

Conclusion

5. **This action is made final.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire in three months from the mailing date of this action. In the event a first reply is filled within two months of the mailing date of this final action and the advisory action is not mailed until after the end of the three-month shortened statutory period, then the shortened statutory period will expire on the date of the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than six months from the date of this final action.

Contact Information

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chengyuan Tseng whose telephone number is (571)272-9772, and fax number is (571)273-9772. The examiner can normally be reached on Monday through Friday from 09:00 to 17:00. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dr. Henry Tsai can be reached on (571)272-4176. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/CT/

Patent Examiner, AU 2184

/Henry W.H. Tsai/

Supervisory Patent Examiner, Art Unit 2184